## ABSTRACT

An improved low voltage to high voltage translator for digital electronic circuits providing reduced rise times, fall times and transition times that remain independent of operating conditions. This is accomplished by modifying a conventional low-to-high voltage translator to include a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator and a switched active pull-down at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so as at to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.